Wire Crystals of GaAs and InAs Grown by Molecular Beam Epitaxy on Porous Silicon

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Undoped and Si doped GaAs and InAs films on porous Si were grown by molecular beam epitaxy at different substrate temperatures T_s = 200, 300, 400 and 500°C. The dependence of the surface morphology on the growth conditions has been investigated. The possibility to grow GaAs wire crystals with lengths of 120 μm and diameter between 75 and 100 nm has been demonstrated. We propose two possible mechanisms of growth. The first mechanism we suggest is the anomalous long diffusion length of Ga adatoms on the lateral surface of the growing crystals. The second possible mechanism is the existence of associates and micro-clusters of Ga and As atoms on the surface semiadsorbtional layer. In this case the crystal growth process can be described by the vapor-semiadsorbtional layer-solid scheme. The heterojunction diodes of Si-doped GaAs on porous Si were produced and I-V characteristics at 77K are shown.

I. Introduction

Recently the significant progress of technology gave rise to the intensive investigations of optical and transport properties of one and zero-dimensional systems[1-3]. Two basic methods have been developed for fabrication of such systems: i) epitaxial growth of two-dimensional structure and treatment of microclusters by re-crystallization or selective etching[4], ii) fabrication of quantum dots and wires by combination of MBE, plasma etching and electron lithography[5-6] or by growth on the semiconductor's lateral and faceting surfaces[7-8], when the low-dimensional structure was produced by monolayer overgrowth.

In this work, the mechanism of GaAs growth on porous Si has been investigated using the scanning electron microscope (SEM), and eletrical properties of Si-doped GaAs on porous silicon.

II. Experiment

The substrates used were < 111 > oriented, 10 Ω cm resistivity, boron-doped, p-type silicon. The anodization was carried out using 25% HF solution in H_2O, at current density of 30mA/cm^2 for 5 min. After etching, wafers were rinsed in ethanol and dried in ambient air. All samples exhibited visible pliotolurninescence a.t 300K.

After electrochemical preparation the porous silicon was bonded by Iii on a molybdenum block and loaded in the lock-in lock system of MECA 2000 MBE installation. The interval between tlie end of the cheniical preparation and the substrate transfer to ultra high vacuum was 30-40 min for the minimization of porous Si oxidation. Thc epitaxial layers were prepared in two steps. These start by heating the porous silicon (PS) under Ga fiux for 2 min at 750°C in order to desorb the native oxide. Afterwards the Ga shutter was closed, and the heating process coiitinued for 20 min to evaporate tlie Ga metal. The substrate temperature Ts is then lowered and the first step was initiated by depositing a 0.2 μm buffer layer of GaAs at 200°C with growtli rate 0.1 μm/h, followed by a 5 min annealing at 550°C under As flux. Then the deposition procedure was executed under As-stabilized coiiclitions at a growth rate of 1/μ/h during 1/2 h. A similar process was done for the InAs growth.

The current-voltage (I - V) characteristics of GaAs/PS heterojunction diodes were measured at 300 and 77K. Electrical contacts were produced by conventional thermal indium evaporation, using a shadow mask. After evaporation the contacts were alloyed in

nitrogen atmosphere at 350°C during 3 minutes. The contact area is about 1.0 mm.

The produced diode shows retification characteristics in vertical transport between silicon substrate and n-layer GaAs. We observe an increase in the value of current when the temperature is changed to 77K. The I-V results of one such heterojunction diode are shown in Fig. 1, for 77K.

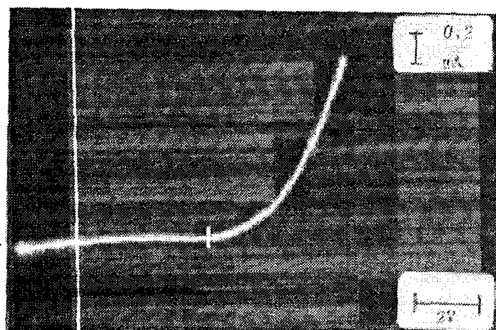

Figure 1: I-V characteristics of the GaAs/PS heterojunction diodes at 77K.

The forward "turn-on" voltage is about 0.8V in the GaAs/PS heterojunction diodes produced, and leakage current for voltages smaller than 4 V is not observed.

III. Results and discussion

The surface structure of the porous Si at low magnification in tlie scanning electron microscope is shown in Fig. 2.

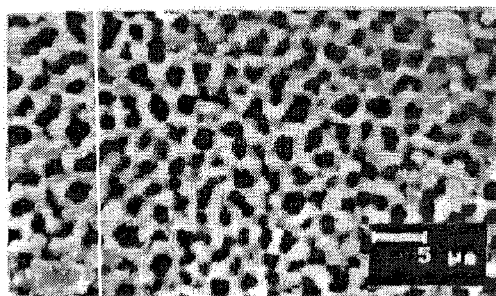

Figure 2: Layer structure of porous silicon.

Fig. 3 shows the surface morphology of the epitaxial GaAs layers at substrate temperatures of 400°C. The layers grown at 200 and 380°C have a similar friable amorphous structure. In this temperature range, increasing T_s to 380°C gave rise to the roughness increase of the surface.

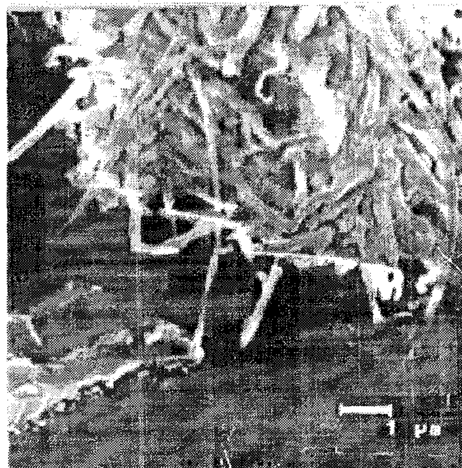

Figure 3: Surface morphology of GaAs/PS growth at 400°C.

At 400° the surface structure transforms into small crystals and we can see growth of the single crystal wires of GaAs with, furthest from the surface, a. diameter of around 100 nm and about 5μm length. The growth rate 0.1 $\mu m/h$ was determined from the parallel growth process using RHEED oscillations, and as we can see tlie length of a wire crystal in Fig. 1 is about 10 times bigger than the one obtained in the parallel growth.

Fig. 4 shows surface fragments with 120 μm length crystals. The wire diameter is ~80nm. The growth mechanism was not changed qualitatively with increase of T_s to 500°C. Tlie layer grown at this temperature lias similar structure to the sample grown at T_s = 400°C, however tlie size of the small crgatallites was slightly enlarged. The GaAs crystal wire diameter augmented aiid tlie length-wise shortened into whiskers.

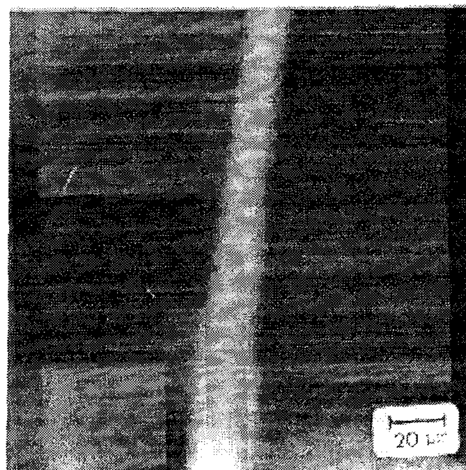

Figure 4: Fragment of GaAs/PS *surface* with wire crystals of length 120/μm.

Figure 5: Fragment of InAs/PS surface with crystals of length $100 \mu m$.

Fig. 5 shows surface fragments of InAs/PS with 77nm diameter crystals. Tlie highest crystal density is located on the crack borders, wliicli. cross the surface of InAs porous Si islands, i.e. the epitaxial growth of InAs begins in an area of plastic deformation. For more precise determination of tlie temperature for which the growth mechanism is changed we investigated series of samples grown between T_s = 380, 420 aiid 440°C. We found tliat this mechanism was changed at T_s = 400+10°C; tlie layer which was grown at 380°C demonstrated friable disordered surface, however at 400°C the crystal wires were observed. At T_s = 400°C the crystals diameter size increases and the wires tend to be shorter.

Tlie growth process of whiskers by MBE on III-V materials was investigated[9] using tlie vapor-liquid-solid (VLS) mechanism. This regime of growth was realized by MBE under conditions of stabilization of growth surfaces by IIIa group element. Tlie RHEED pattern during growth in this regime shows well known metal-stabilized surface structure with tlie complete saturation of the top monolayer by metal adatoms. When GaAs film is grown by MBE, the Ga atoms have a sticking coefficient ~1. The atonis of Ga which are not incorporated into the lattice, were collected into micro droplets on the surface growing layer. From tlie saturation of tliese droplets by the vapor phase of As tlie whiskers begin to grow by tlie VLS mechanism, as described in Ref.[10].

In our experiments, as we indicated above, the ratio of the As/Ga fluxes was in concordance with rich arsenic conditions, tlierefore Ga droplet formations on the surface was not possible. From this we conclude that the growth mechanism of GaAs wire crystals on porous Si are completely different from tlie mechanism described ill Ref.[10].

Tlie second possible mechanism can be explained by Ga and As atom transport to the wire tops through the existence of a.thick semiadsorbtional layer of Ga and As adatoms on the surface of the GaAs a.t low temperature T_s. At the lower temperature conditions (T_s = 400°C), the surface of GaAs layer lias an over monolayer ordered coverage of As adatoms with the As-stable (2×2) structure and an additional nuinber of adsorbed As atoms in a.disordered phase. Therefore we suggest that at low temperature tlie surface kinetics of atom incorporation clecreases, resulting in tlie appearance of semiadsorbtional layers with Ga and As clusters. This layer on tlie solid surface is similar to tlie saturated metal liquid phase, and crystal growth in this case is governed by the vapor-semiadsorbtional solid layer growth mechanism. Wire growth breakdown a.t temperature T_s below 380°C can be explained by the first model.

In summary, a.new possibility for tl-ie formation of GaAs wire crystals by MBE on porous Si has been demonstrated. It was found that the optimum temperature is 400°C, witli a wire length of 120 μm and diameter near to 75-100 nm. These nanocrystals were observed in the microcracking area of a GaAs layer on porous Si. We believe tliat tlie germ formation of nanocrystals begins on the output of the dislocations on tlie GaAs growing layer. Two meclianisms of wire crystal growth in tlie absence of metal liquid solution on the epitaxial layer surface have been discussed. For the first mechanism we suppose the long diffusion length of Ga adatoins along the lateral surface is responsible for the wire growth. As tlie second mechanism, we suggest a thick seiniadsorbtional layer of Ga and As results by transport of Ga and As atoms to tl-ie wire tops.

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